NAME :KRISHMA BHATIA

DEPARTMENT:COMPUTER ENGINEERING DESIGNATION: LECTURER

SEMESTER:4TH

SUB:COMPUTER ORGANIZATION

TEACHING LOAD:3(L) March 2023-June 2023

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| WEEK  NO. | THEORY DAY | TOPICS COVERED |
| 1 | 1 | Hardware organisation of Computer system |
| 2 | CPU organisation : general register organisation, stack organisation |
| 3 | Instruction formats :three address, two address, one address, zero address |
| 2 | 1 | RISC instruction |
| 2 | Addressing modes Introduction |
| 3 | Immediate, register, direct, in direct Addressing modes |
| 3 | 1 | Relative, indexed Addressing modes |
| 2 | CPU Design : Micro programmed vs hard wired control |
| 3 | CISC characteristics |
| 4 | 1 | Reduced instruction set computers, RISC characteristics |
| 2 | Comparison between RISC AND CISC |
| 3 | Assignment 1 |
| 5 | 1 | Memory organization Introduction |
| 2 | Memory Hierarchy |
| 3 | RAM and ROM chips, Memory address map, Memory connections to CPU |
| 6 | 1 | Auxiliary memory Magnetic disks and magnetic tapes |
| 2 | Associative memory ,Cache memory, Virtual memory |
| 3 | Memory management hardware |
| 7 | 1 | Read and Write operation |
| 2 | Revision |
| 3 | Assignment 2 |
| 8 | 1 | I/O organization |
| 2 | Basis Input output system(BIOS) |
| 3 | Function of BIOS |
| 9 | 1 | Testing and initialization |
| 2 | Configuring the system |
| 3 | Modes of Data Transfer |
| 10 | 1 | Programmed I/O : Synchronous, asynchronous and interrupt initiated |
| 2 | DMA data transfer |
| 3 | Assignment 3 |
| 11 | 1 | Architecture of multi processor systems |
| 2 | Forms of parallel processing |
| 3 | Parallel processing and pipelines, basic characteristics of multiprocessor |
| 12 | 1 | General purpose multiprocessors |
| 2 | Interconnection networks : time shared common bus, multi port memory |
| 3 | Cross bar switch, multi stage switching networks and hyper cube structures |
| 13 | 1 | Test |
| 2 | Revision |
| 3 | Revision |
| 14 | 1 | Revision |
| 2 | Revision |
| 3 | Test |